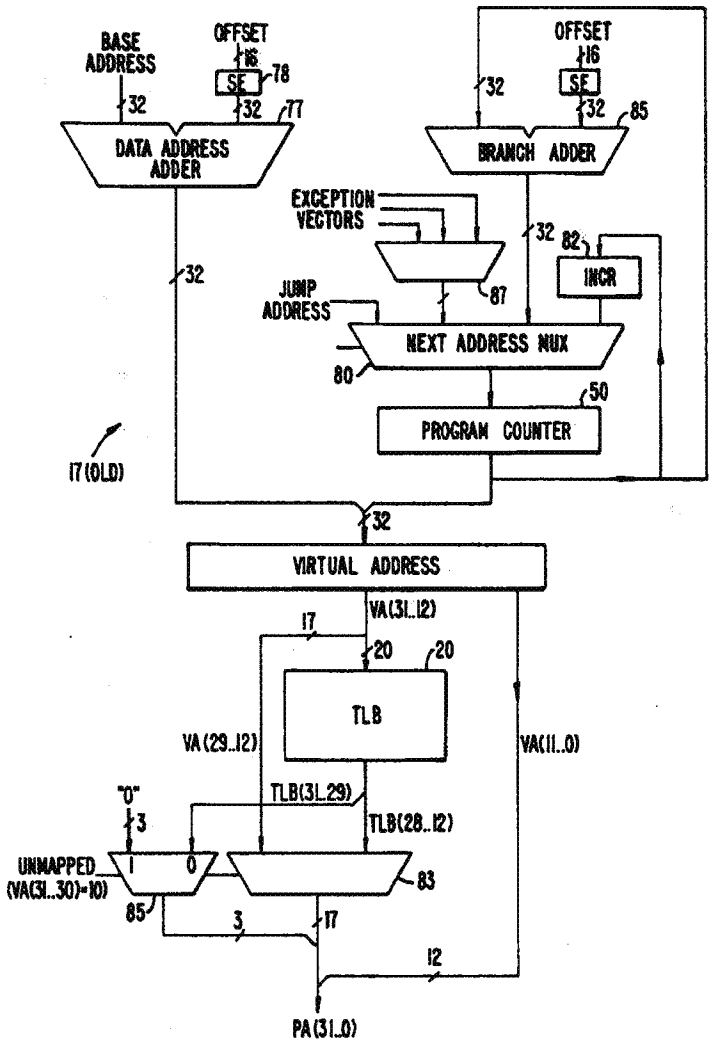

FIG. 3C. (PRIOR ART)

A sign-extension circuit 78 sign-extends a 16-bit offset to 32 bits before the offset is combined at an adder 77 (col. 11, lines 44-46). Moreover, a branch adder 85 combines content of a program counter 50 (PC) and an offset derived from a 16-bit immediate field in a branch instruction (col. 11, lines 62-64).

Applicant respectfully submits that Killian does not disclose or suggest a processor as recited in claim 1. For example, Killian does not disclose or suggest "the single piece of common subcircuitry configured to perform sign extensions of an immediate field in the non-branch instructions and to be reused to perform sign extensions of an immediate field having units of bytes in the branch instructions to calculate a target address for the branch instructions,

wherein said common subcircuitry operating on the non-branch instructions is the same subcircuitry operating upon the branch instructions" combined with the remaining recitations of claim 1. For example, the specification describes on page 11, lines 6-19:

> Although both the branch instruction and the add integer instruction perform sign extension operations on the immediate field value, the branch instruction multiplies the immediate field value by four before performing the sign extension. The multiplication is performed to allow for word alignment and an expanded target branch address range. However, by requiring a multiplication of four before performing the sign extension, different subcircuitry route is required to perform the operation. In many instances, one subcircuit is specifically configured to sign extend an immediate field and another subcircuit is specifically configured to perform a sign extend of an immediate field multiplied by four. In some examples, multiplication by four is performed by using additional multiplexers and shifters on a base sign extended subcircuit. However, having additional hardware or additional subcircuits is expensive, particularly for programmable chips. Consequently, and the techniques and mechanisms of the present invention allow the reuse of subcircuitry for both types of instructions.

Rather, Killian discloses two different sign extension circuits to perform sign extensions. As shown above in Figure 3C, there are two different sign extension circuits, one numbered 78 and the other one is not numbered. Furthermore, the sign extension circuit 78 sign-extends a 16-bit offset to 32 bits before the offset is combined at an adder 77 and the other sign extension circuit (not numbered) sign extends another 16 bit offset to 32 bits. There is no disclosure or suggestion in Killian of "the single piece of common subcircuitry configured to perform sign extensions of an immediate field in the non-branch instructions and to be reused to perform sign extensions of an immediate field having units of bytes in the branch instructions to calculate a target address for the branch instructions". Hence, for at least the reasons set forth above,

Applicant respectfully submits that claim 1 is not anticipated by Killian.

Additionally, the presently pending dependent claims 2-8 are not anticipated by Killian because they depend upon independent claim 1.

Hence, for at least the reasons set forth above, Applicants respectfully request that the Section 102 rejection of claims 1-8 be withdrawn.

Section 103 Rejection

Claims 14-19, 31, and 32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Killian in view of Wittig et al., "OneChip: An FPGA Processor with Reconfigurable Logic" ("Wittig"). Applicant respectfully traverses this rejection.

For at least the same reasons set forth above, Killian does not disclose or suggest "the single piece of common subcircuitry performs a sign extension of the immediate field associated with the one of the branch instructions and that is reused to perform a sign extension of the immediate field associated with the one of the non-branch instructions, wherein said common subcircuitry operating on the non-branch instructions is the same subcircuitry operating upon the branch instructions" combined with the remaining recitations of claim 14. Moreover, Wittig is not cited to cure the deficiencies stated above in Killian. Rather, as stated in paragraph 14 of the Office Action, Wittig is cited to teach a field programmable gate array. Hence, for at least these reasons, claim 14 are not obvious over the combination of Killian and Wittig.

Additionally, the presently pending dependent claims 16-19, 31, and 32 are not obvious over the combination of Killian and Wittig since they depend upon independent claim 14.

Hence, for at least the reasons set forth above, Applicants respectfully request that the Section 103 rejection of claims 14-19, 31, and 32 be withdrawn.

Conclusion

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. Should the Examiner believe that a telephone conference would expedite the prosecution of this application; the undersigned can be reached at the telephone number set out below.

Please charge any required fees or credit any over payments to Weaver Austin Villeneuve Sampson LLP deposit account 504480.

Respectfully submitted,

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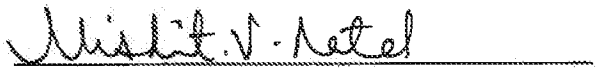
Respectfully submitted,



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